

Form PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. 60,408-126		SERIAL NO.								
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		APPLICANT: Fruehling et al.										
		FILING DATE		GROUP:								
U.S. PATENT DOCUMENTS												
Examiner Initial	Document No.		Date	Name	Class	Sub- Class	Filing Date					
MS	5	1	9	3	1	8	9	03/09/93	Flood et al.	395	650	12/09/91
	5	4	0	4	3	0	4	04/04/95	Wise et al.	364	426.04	11/19/93
	5	4	5	9	7	3	2	10/17/95	Wise et al.	364	426.02	11/19/93
	5	8	2	5	7	8	5	10/20/98	Barry et al.	371	22.4	5/24/96
	5	8	4	1	8	6	7	11/24/98	Jacobson et al.	380	25	11/01/96
	6	0	0	6	3	4	5	12/11/99	Berry Jr.	714	718	05/09/97
	6	0	6	5	1	3	5	05/16/00	Marshall et al.	714	11	06/04/99
	6	1	7	0	0	2	5	01/02/01	Drott et al.	710	48	08/11/98
FOREIGN PATENT DOCUMENTS												
Examiner Initial	Document No.		Date	Name	Class	Sub- Class	Filing Date					
OTHER DOCUMENTS (Incl. Author, Title, Date, Pertinent Pages, etc.)												
AA	J. Sosnowski, Concurrent Error Detection Using Signature Monitors. Proc of Fault Tolerant											
MS	Computing Systems, Methods, Applications. 4th International GI/ITG/GMA Conference,											
	Sept. 1989, pp 343-355											
AB	K. Wilken, J.P. Shen, "Continuous Signature Monitoring: Low-Cost Concurrent Detection											
MS	of Processor Control Errors, "IEEE Transactions on Computer-Aided Design, Vol. 9, pp. 629-641											
	June 1990.											
AC	Intel Corporation, Embedded PentiumR Processor Family Developer's Manual, "Error											
MS	Detection," Chapter 22, pp. 393-399											
Examiner				Date Considered 10/6/05								
Examiner: Initial if references considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.												

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Examiner Initial	Document No.			Date	Name	Class	Sub- Class	Filing Date
OTHER DOCUMENTS (Incl. Author, Title, Date, Pertinent Pages, etc.)								
AD nd	E. Bohl, T. Lindenkreuz, and R. Stephan, "The Fail-Stop Controller AE11, "Proc. International Test Conference, IEEE Computer Society Press, Los Alamitos, Calif., 1997, pp. 567-577							
AE nd	U.S. Patent Application "METHOD AND CIRCUIT FOR ANALYSIS OF THE OPERATION OF A MICROCONTROLLER USING SIGNATURE ANALYSIS OF MEMORY".							
	Serial No.: 09/309,055 Filed May 10, 1999							
AF nd	U.S. Patent Application "METHOD AND CIRCUIT FOR ANALYSIS OF THE OPERATION OF A MICROCONTROLLER USING SIGNATURE ANALYSIS OF DATA AND INSTRUCTIONS" Serial No.: 09/309,135 Filed May 10, 1999							
AG nd	U.S. Patent Application "METHOD AND CIRCUIT FOR ANALYSIS OF THE OPERATION OF A MICROCONTROLLER USING SIGNATURE ANALYSIS DURING OPERATION							
	Serial No.: 09/309,054 Filed May 10, 1999							
AH nd	DELPHI SECURED MICROCONTROLLER ARCHITECTURE by Terry L. Fruehling, SAE 2000 World Congress, March 6-9 2000, pp.1-12							
Examiner	[Signature]			Date Considered	10/6/05			